ANNEX A

PUBLIC SELECTION BASED ON QUALIFICATIONS AND INTERVIEW FOR THE AWARDING OF NO. 1 EXPERIENCED GRANT LASTING 13 MONTHS FOR CONDUCTING RESEARCH PURSUANT TO ART. 22 OF LAW NO. 240/2010 AT THE DEPARTMENT OF ENGINEERING AND APPLIED SCIENCES (SC 09/E3 – ELECTRONICS - SSD ING-INF/01 – ELECTRONIC ENGINEERING (CUP: F52F16001350001) TYPE A WITHIN THE FRAMEWORK OF THE 2017/2018 STARS PROGRAMME
PICA CODE 20AR005

announced with decree of the Chancellor Rep. no. 27/2020 of 16.01.2020 and posted on the official registry of the University on 23.01.2020

RESEARCH PROJECT

"Intelligent microelectronic systems for a new generation of silicon pixel detectors"

Research structure: Department of Engineering and Applied Sciences
Duration of the grant: 13 months
Scientific Area: 09 – Industrial and information engineering
Academic recruitment field: 09/E3 – Electronics
Academic discipline: ING-INF/01 – Electronic Engineering
Scientific Director: Prof. Valerio Re

The project involves the study of new microelectronic systems for the readout of pixel sensors used in the Large Hadron Collider (LHC) at CERN in Geneva and in future accelerators.
The experiments at LHC have achieved extremely interesting results in the field of high energy physics, among which the discovery of the Higgs boson stands out. The performance of LHC has improved over the years in terms of energy and luminosity, and will reach an ultimate limit in the next decade, in order to increase the potential of new discoveries related to crucial scientific issues, such as the nature of dark matter and the existence of supersymmetric particles. These extreme operating conditions, as well as those envisaged for future accelerators beyond LHC, require particle detection systems with a performance never previously achieved in terms of spatial, temporal, and energy resolution. These performances will be largely entrusted to the use of the most recent microelectronic technologies for the readout of the signals generated by the particles in the detectors, in particular in the silicon pixel sensors positioned closer (some cm) to the region where the beams collide giving rise to the physics events studied by the experiments.
In the next decade at LHC, pixel readout microelectronic circuits will have to amplify small signals with excellent noise behavior and radiation resistance, and will have to process an extremely large amount of data. Complex electronic functions will be implemented with a very high integration density, as dictated by the need of acquiring signals from pixel sensors with a pitch of a tens of a μm.
This project aims to experimentally test a 65 nm CMOS integrated circuit for the readout of the silicon pixel detectors of the CMS experiment at LHC. Moreover, the project foresees the evaluation of an even more scaled CMOS technology (28 nm) in view of applications of this type of detectors for the tracking of particles in future colliders. Finally, it is also planned to evaluate the use of these recent-generation microelectronic technologies (65 nm and 28 nm) for the readout of monolithic pixel sensors. In this case the analog front-end will be integrated into the pixels of the sensor, while the integrated readout circuit will include the analog-to-digital converters and the digital readout architecture of the pixel matrix.
The project will be structured in three stages:
1) Experimental tests on the integrated circuit in 65 nm CMOS technology for the pixel detectors at LHC (6 months).
2) Development of the design of analog and digital circuits resistant to radiation in CMOS 28 nm technology with innovative solutions for processing signals from pixel detectors (3 months)
3) Development of the design of a system based on monolithic pixel sensors and digital integrated readout circuits (4 months)